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(54) NMOS LOW CONCENTRATION DRAIN AND PMOS HALO IC PROCESS FOR CMOS TRANSISTOR

(57) Abstract:

PURPOSE: To provide a new 'architecture' and structure for the source and drain regions of a CMOS transistor, using an N⁻LDD layer and an N⁻LDD introduction sequence for both NMOS and PMOS transistors.

CONSTITUTION: A polygate is used for a self-aligned transistor SAT mask, and an N-type dopant material with a relatively low dosage is introduced into the source and drain regions of a CMOS transistor. A low concentration N-type LDD layer N⁻LDD is formed in the source and drain region of an NMOS transistor, and a low concentration N-type halo layer PHLDD is formed in the source and drain regions of a PMOS transistor.